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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,948	03/19/2004	Makoto Kudo	118767	7180

25944 7590 08/07/2006

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EXAMINER	
ZAMAN, FAISAL M	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 08/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,948	KUDO, MAKOTO	
	Examiner	Art Unit	
	Faisal Zaman	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/04, 5/24/05, 5/31/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-8** are rejected under 35 U.S.C. 102(b) as being anticipated by Sugimoto (U.S. Patent No. 5,850,541).

Regarding Claims 1, 3, and 7, Sugimoto discloses a semiconductor device (Figure 1, item 100) that accesses at least one semiconductor storage medium (Figure 1, item 106), comprising:

A bus master (Figure 1, item 101);

A bus interface (Figure 1, item 105b) that controls access to the at least one semiconductor medium based on a request for access to the least one semiconductor storage medium from the bus master (Figure 1, item 102, Column 6, lines 10-19);

A clock-supply-control circuit that controls the presence of the supply of a clock to the bus master based on access state information that indicates a state of access to the at least one semiconductor storage medium, the clock-supply-control circuit including a circuit that implements at least one of control for stopping the supply of the clock to the bus master if the circuit determines that the bus interface is at a BUSY state (Column 6, lines 20-30; ie. if bus control unit

[BCU] 105 is busy, it inactivates the clock signal to CPU 101), and control for supplying the clock to the bus master if the circuit determines that the bus interface is at a non-BUSY state, based on the access state information (Figure 1, item 105c, Column 6, lines 5-9 and lines 46-51; ie. clock control section 105c suspends the clock signal until data to be written to CPU 101 is ready [e.g. it receives the ready signal 109 from the storage device 106).

Regarding Claims 2, 4, and 8, Sugimoto discloses wherein the clock-supply-control circuit implements a processing to stop the supply of the clock to the bus master after completion of a request output from the bus master (Figure 3G and 3H, Column 6, lines 46-51; ie. after CPU 101 makes a read request, the clock signals 1054 and 112 are suspended until the data is ready to be written to CPU 101 from storage device 106).

Regarding Claims 5 and 6, Sugimoto discloses electronic equipment, comprising:

A semiconductor device that includes the semiconductor device according to Claim 1 (Figure 1, item 100);

A receiving device that receives input information; and an output device that outputs a result processed by an information-processing device based on the input information (Figure 1, item 107, Column 5, lines 26-33 and 48-52; ie. peripheral function 107 performs input/output processing).

Prior Art of Record

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jain et al. (U.S. Patent No. 5,586,332 A) discloses power management for low power processors through the use of auto clock-throttling. Sezaki et al. (U.S. Patent No. 6,601,131 B2) discloses flash memory access control via clock and interrupt management. Kawahara et al. (U.S. Patent No. 6,751,741 B1) discloses a computer power management apparatus and method for optimizing CPU throttling. Takamiya et al. (U.S. Patent No. 6,990,599 B2) discloses a method and apparatus of clock control associated with read latency for a card device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

fmz

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
8/3/06